MICHAEL TECHNOLOGY
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SUMMARY

Senior Hardware/Software/System Engineer. Solid background in delivering successful on-time solutions in hardware, software and systems engineering disciplines with expertise in Digital Hardware Design, FPGA Design, Windows Software Design, Design for Test, Test Equipment Design and Environmental Testing. Works well with multiple competing priorities in a team environment. Experience in leading small groups. Previously held top secret clearance.

COMPUTER LANGUAGES/TOOLS

- VHDL (5+ years)
- C++ (10+ years)
- Xilinx ISE (CoreGen, ChipScope)
- Microsoft Visual C++
- Synplicity Simplify Pro
- Gnu C++
- ModelSim
- National Instruments Lab Windows
- Lattice ispLever
- Logic Analyzers (Tek and HP)
- Emulators(EIP, BDM)
- JTAG Tech Software Tools

PROFESSIONAL EXPERIENCE

HONEYWELL INC, Air Transport/Business Jet Div, Phoenix, AZ **1993-2005**

Principal Electrical Engineer
Responsible for the development of a PCI based hardware simulations card used by software test teams and flight simulator customers as an inexpensive substitute for actual flight hardware. Selected to find a solution for a project that was several months behind schedule. The projects completed on schedule.

Achievements:
- Provided a prototype early which allowed the program to complete on schedule.
- Reduced state machines states and improved timing to achieve a greater than 2 to 1 simulation to real time ratio. Goal was to achieve a 1 to 1 simulation to real time ratio.
- Created a software path coverage "function" to replace a similar tool valued at the total recurring cost of this device.
- Designed the CCA, FPGA, Embedded tests and PC hosted test. Task included parts selection, architecture design, designing hardware, and writing test. Used a Xilinx Spartan II FPGA, Synplicity Simplify, Xilinx IDE and ModelSim. There were two generations; a version based on a 32MHz AMD29050 and one on a 64MHz AMD29050 derivative. Test Software was written in MSVC++.

Responsible for the development of a Boundary Scan software tool for use by production hardware. This included providing a solution for data loading capability on a critical program. The Software is now being used by all new major hardware programs at this division.

Achievements:
- Reduced the initial program risk by prototyping the software and flushing out the requirements prior to integration on engineering development hardware. There was zero integration time when the product was made available for integration.
- Provided a high level interface to the IEEE1149.1 and IEEE1169.5 buses and also provided low level control for diagnostic capabilities.
- Ported Software to 3 platforms; Embedded (gcc), PC Unix (gcc) and windows (MSvc++).
- Developed a hardware interface using VHLD for a PLD to increase load times by a factor of 8 reducing load times on one application from approximately ½ hour to around 3 minutes.

Responsibilities for the development of hardware test software for a program that had a late start in providing an integration solution to a customer. In addition there was a longer term requirement to provide salable test equipment and automated test equipment for production hardware.

Achievements:
- Provided a work-around solution for both in-house and customer integration in France within 4 months of being assigned to project. Sole integrator of solution at the customer site, completing a major program milestone.
- Development an automated test solution that provided diagnostic capabilities written in Lab Windows for the long term solution.
- Supported multiple platforms including coordination with two French partnering companies.
- Lead a team of 5 software engineers in developing embedded test software.

Responsible for the developed a software based emulator interface that replaced an aging hardware emulator for an in-house designed microprocessor for use by software developers, software test engineers and hardware engineers. The emulator was written in National Instruments Lab Windows.

Achievements:
- Provided an emulator containing a disassembler, an inline assembler, built-in data loader, scripting capability and break point capability.
- Developed emulator in time for use on development hardware for a new program.

Responsible for developing an EISA based CCA for a customer of an avionics package who requested a field solution for data loading before accepting the avionics package. Selected to provide the solution.

Achievements:
- Provided the solution on schedule approximately 6 months after program start.
- Designed the CCA and PLD Firmware. The CCA contained a 60MHz ASIC and the PLD was written in ABLE HDL.

Responsible for the development of embedded software to control a PCMCIA (Cardbus) interface.

Achievements:
- Software was used to control an IEEE-488 PCMCIA Card intended to emulate an older system.
- Embedded software written in gnu c++
- Task also included porting older PC software to MSVC++ allowing software to run faster PCs.

Responsible for Technical Leadership of a team of 4 engineers for the development of an ASIC written in VHDL.

Achievements:
- Managed requirements document and code reviews.
- Reduced package size by 50% without reducing functionality reducing overall program risk.
- Arranged for the sale of Intellectual Property derived from the ASIC.

Other tasks include: preformed various product engineering functions including writing hardware Qualifications Test Plans/Reports, Plans for Hardware Aspects of Certification, Test Verification Outline, Testability Analysis, and request for proposals, Technical Reviews and System Analysis. Familiar with CMM, OOA/OOD and VPD (Rapid Prototyping).

EDUCATION:
Bachelors of Science in Electrical Engineering University of Oklahoma, Oklahoma.